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TITLE: Low cost chip size package and method of fabricating the same

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INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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PARENT-CASE:

CROSS REFERENCE TO RELATED APPLICATION This application is a divisional of U.S. patent application Ser. No. 09/326,905, filed Jun. 7, 1999, now U.S. Pat. No. 6,181,569, entitled "Low Cost Chip Size Package And Method Of Fabricating The Same".

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US-CL-ISSUED: 438/612;438/613 ;438/614 ;438/124 ;438/127

US-CL-CURRENT: 438/612; 438/124 ; 438/127 ; 438/613 ; 438/614

FIELD-OF-SEARCH: 438/111; 438/112 ; 438/123 ; 438/124 ; 438/125 ; 438/126

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REF-CITED:

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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ART-UNIT: 2822

PRIMARY-EXAMINER: Picardat; Kevin M.

ABSTRACT:

A first plurality of metal bumps is formed on a semiconductor wafer containing a plurality of chips, each of the first plurality of bumps being in electrical contact with a contact pad on one of the chips. An encapsulant layer is deposited over the first plurality of metal bumps and then polished to expose a top surface on each of the metal bumps. A second plurality of metal bumps is formed on the exposed top surfaces of the first plurality of plurality of bumps, respectively. The wafer is then sawed to separate the individual chips, yielding semiconductor packages which have the same lateral dimensions as the chips. Alternatively, to facilitate the encapsulation process, the wafer can be sawed into rectangular, multi-chip segments before the encapsulant layer is deposited. After the encapsulant layer has been applied and polished and the second plurality of conductive bumps have been formed, the segments are then separated into individual chips. The first plurality of metal bumps can be deposited directly on the contact pads, with or without an underbump metalization layer, or on metal conductive traces over one or more dielectric layers.

7 Claims, 29 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

CLAIMS:

I claim:

1. A method of manufacturing semiconductor chip packages comprising:

providing a semiconductor wafer containing a plurality of chips;

forming a first dielectric layer over a surface of the wafer;

forming a first plurality of holes in the dielectric layer, the holes corresponding with the locations of contact pads on the surface of the wafer;

depositing a first conductive layer on a surface of the first dielectric layer;

patterning the first conductive layer to form traces, each of the traces extending from one of the first plurality of holes;

depositing a second dielectric layer over the first dielectric layer and the first conductive layer;

forming a second plurality of holes in the second dielectric layer, each of the second plurality of holes corresponding with the location of at least one of the traces;

depositing a second conductive layer over the second dielectric layer, the second conductive layer extending into the second plurality of holes;

removing a portion of the second conductive layer, leaving the second conductive layer in the second plurality of holes;

forming a first plurality of conductive bumps in the second plurality of holes;

depositing an encapsulant layer covering the first plurality of conductive bumps;

removing a portion of the encapsulant layer so as to expose a portion of the bumps in the first plurality of bumps; and

forming a second plurality of bumps on the exposed portions of the first plurality of bumps.

2. The method of claim 1 comprising separating the chips by sawing the wafer, the first and second dielectric layer and the encapsulant layer, thereby producing semiconductor chip packages.

3. The method of claim 1 wherein removing a portion of the encapsulant layer comprises polishing the encapsulant layer.

4. A method of manufacturing semiconductor chip packages comprising:

providing a semiconductor wafer containing a plurality of chips;

forming a first dielectric layer over a surface of the wafer;

forming a first plurality of holes in the dielectric layer, the holes corresponding with the locations of contact pads on the surface of the wafer;

depositing a first conductive layer on a surface of the first dielectric layer;

patterning the first conductive layer to form traces, each of the traces extending from one of the first plurality of holes;

depositing a second dielectric layer over the first dielectric layer;

forming a second plurality of holes in the second conductive layer, each of the second plurality of holes corresponding with the location of at least one of the traces;

depositing a second conductive layer over the second dielectric layer, the second conductive layer extending into the second plurality of holes;

removing a portion of the second conductive layer, leaving the second conductive layer in the second plurality of holes;

forming a first plurality of conductive bumps in the second plurality of holes;

sawing the wafer into segments, at least one of the segments containing a plurality of chips;

depositing an encapsulant layer covering the first

plurality of conductive
bumps in said at least one segment;

removing a portion of the encapsulant layer so as to expose a portion of the
bumps in the first plurality of bumps; and

forming a second plurality of bumps on the exposed portions of the first
plurality of bumps.

5. The method of claim 4 comprising separating the chips by sawing the
segment, thereby producing semiconductor chip packages.

6. A method of manufacturing semiconductor chip packages comprising:

providing a semiconductor wafer containing a plurality of chips, each of the
chips having a plurality of contact pads;

depositing a dielectric layer over the wafer;

forming a plurality of holes in the dielectric layer, each of the holes
corresponding with the location of at least one of the contact pads;

depositing a conductive layer over the dielectric layer, the conductive layer
extending into the holes;

removing a portion of the conductive layer, leaving the second conductive layer
in the holes;

forming a first plurality of conductive bumps in the plurality of holes;

depositing an encapsulant layer covering the first plurality of conductive
bumps;

removing a portion of the encapsulant layer so as to expose a portion of the
bumps in the first plurality of bumps; and

forming a second plurality of bumps on the exposed portions of the first
plurality of bumps.

7. A method of manufacturing semiconductor chip packages comprising:

providing a semiconductor wafer containing a plurality of chips, each of the
chips having a plurality of contact pads;

forming a first plurality of conductive bumps in electrical contact with the
contact pads, respectively;

depositing an encapsulant layer covering the first plurality of conductive
bumps;

removing a portion of the encapsulant layer so as to expose a portion of the
bumps in the first plurality of bumps; and

forming a second plurality of bumps on the exposed portions of the first
plurality of bumps.

	U	1	2	3	Document ID	Issue Date	Pages
1	☒	☐	☐	☐	US 6350668 B1	20020226	19
2	☐	☐	☐	☐	US 6110537 A	20000829	12
3	☐	☐	☐	☐	US 4960614 A	19901002	24
4	☒	☐	☐	☐	US 4803124 A	19890207	9
5	☒	☐	☐	☐	US 4313995 A	19820202	6
6	☐	☐	☐	☐	US 4091125 A	19780523	6

	Retrieval Classif	Inventor	S	C	P	Image Doc. Displayed	PT
1		Chakravorty, Kishore K.	☒	☐	☐	US 6350668	☐
2		Heffner, Kenneth H. et al.	☒	☐	☐	US 6110537	☐
3		Durand, David	☒	☐	☐	US 4960614	☐
4		Kunz, Rene	☐	☐	☐	US 4803124	☐
5		Delgadillo, Joseph A.	☐	☐	☐	US 4313995	☐
6		Delgadillo, Joseph A.	☒	☐	☐	US 4091125	☐

	Title	Current OR	Current XRef
1	Low cost chip size package and method of fabricating the same	438/612	438/124; 438/127; 438/613; 438/614
2	Coating integrated circuits using thermal spray	427/448	427/446; 427/96
3	Printed circuit board	427/511	204/155; 427/510; 427/96; 522/1; 522/14; 522/4; 522/81; 522/96
4	Bonding semiconductor chips to a mounting surface utilizing adhesive applied in starfish patterns	428/200	118/411; 156/295; 156/299; 156/578; 228/33; 239/601; 29/832; 29/840; 427/96
5	Circuit board and method for producing same	428/201	156/253; 156/261; 427/259; 427/275; 427/292; 427/96; 428/195; 428/209; 428/320.2; 428/432; 428/901
6	Circuit board and method for producing same	427/96	156/153; 156/247; 156/250; 427/259; 427/385.5; 427/386; 427/409; 427/410